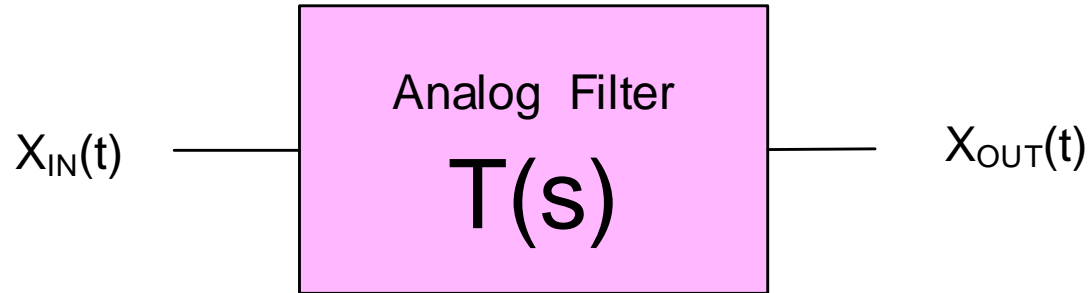


EE 508 Lecture 38

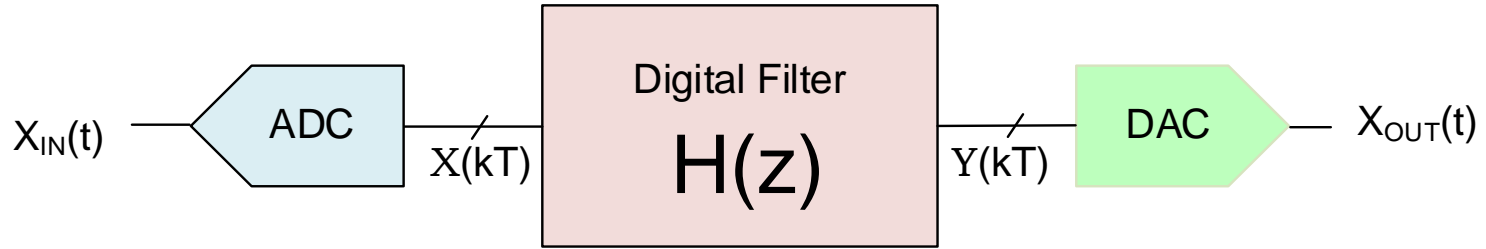
Digital Filters

Review from last lecture

Analog vs Digital Filter



Digital Filter Properties



Theorem: Any FIR filter is linear phase if the impulse response is symmetric or antisymmetric

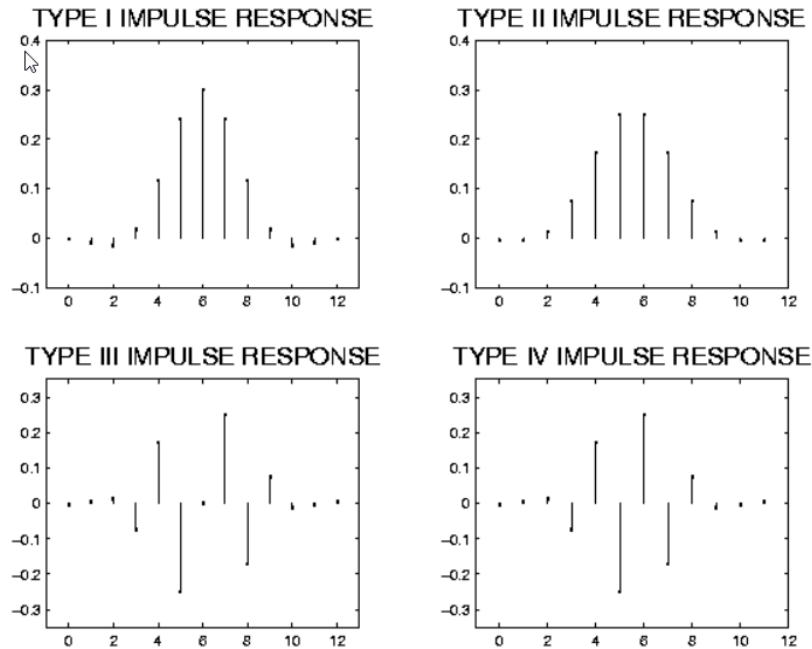
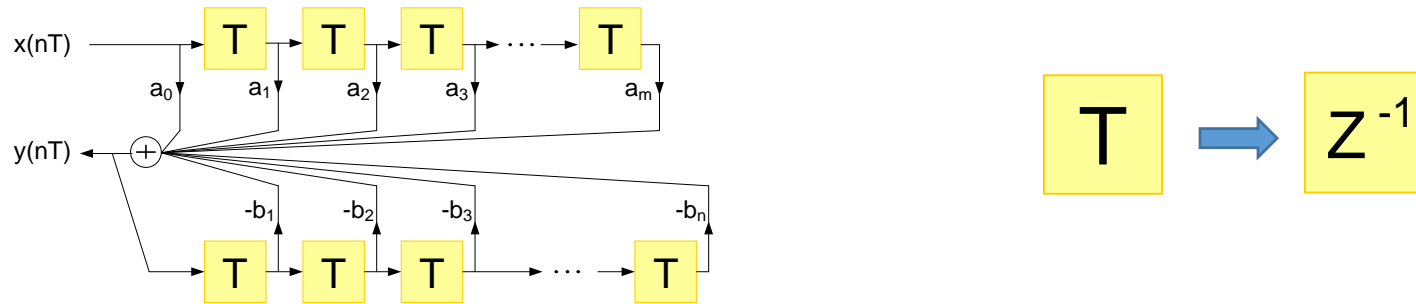


Figure 1

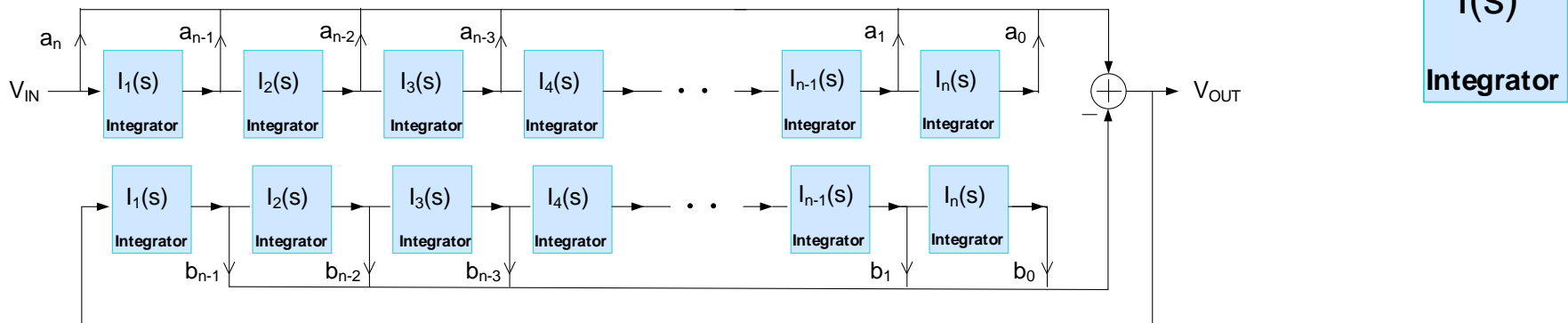
Table from Robert Novak book

Review from last lecture

An Implementation of a Digital Filter



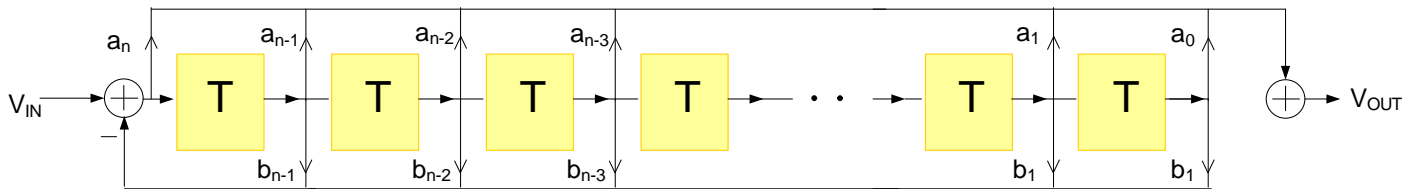
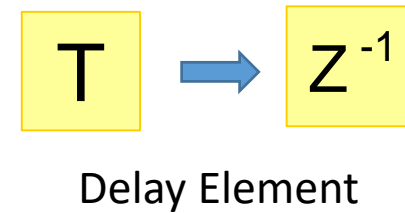
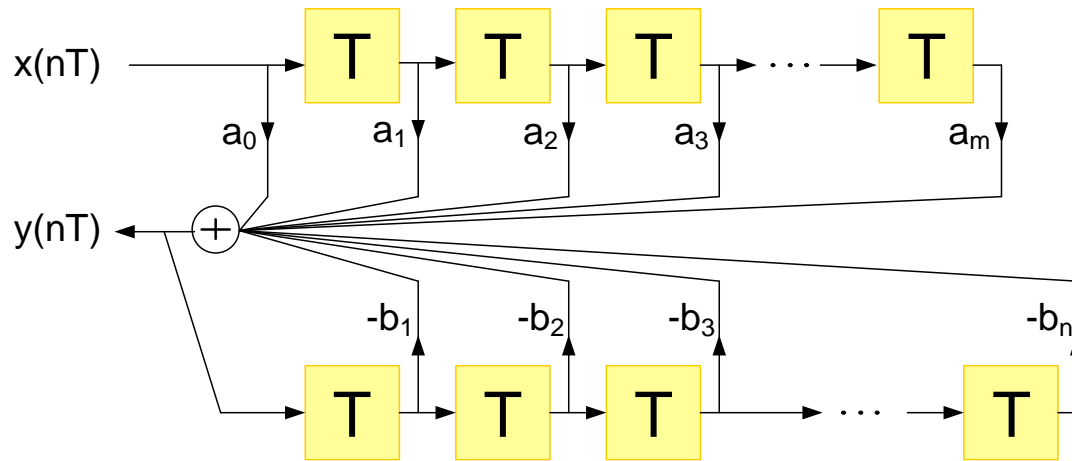
An Implementation of an Analog Filter



- Can be viewed as analogous implementations
- Neither particularly practical
- Many other architectures for both analog and digital filters
- Approximately double the number of integrators or delay elements needed

Review from last lecture

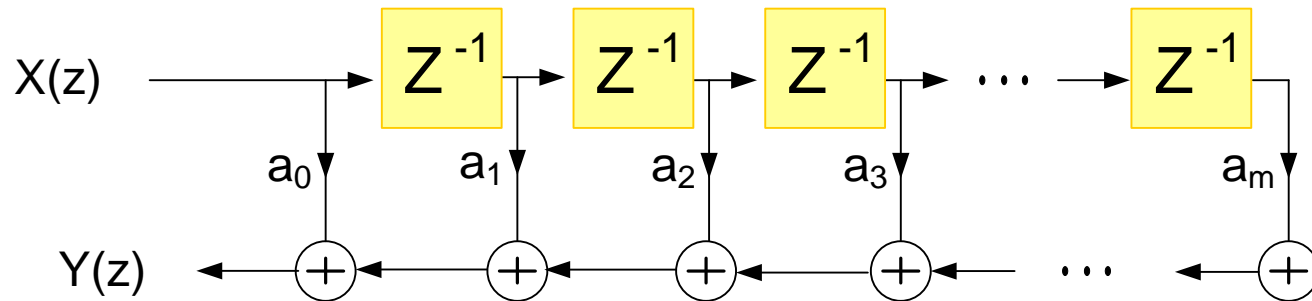
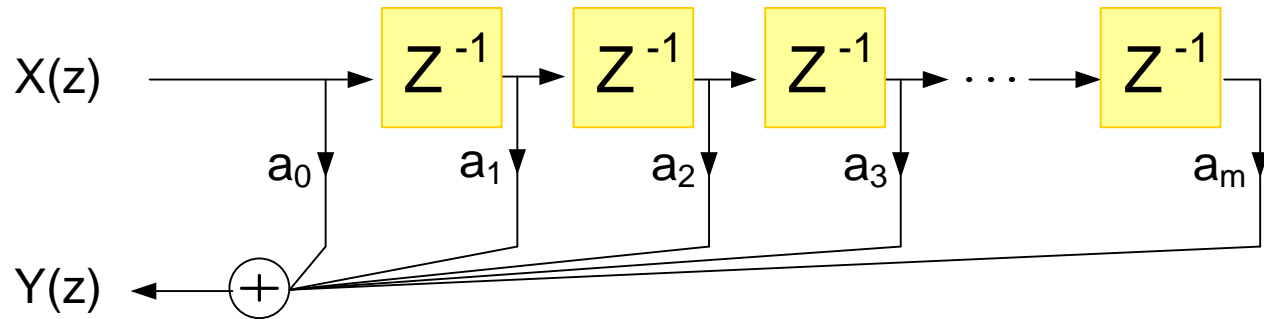
Alternate Implementations of an Digital Filter



- Reduced number of delay elements by factor of 2
- Still not particularly practical
- Similar architectural change can be made for analog filter (next slide)

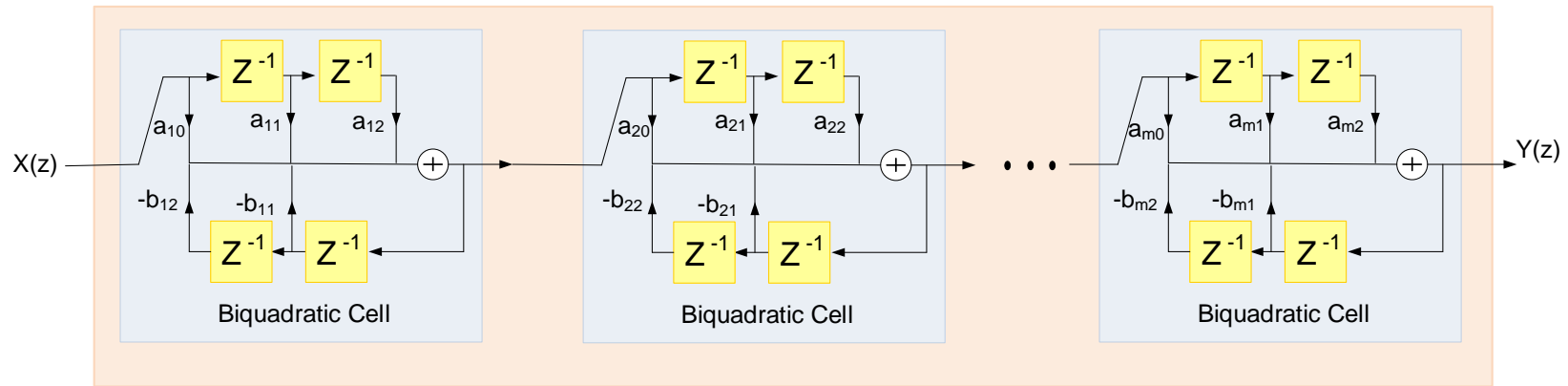
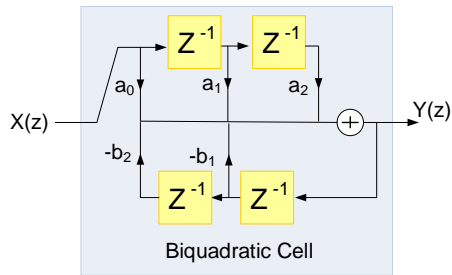
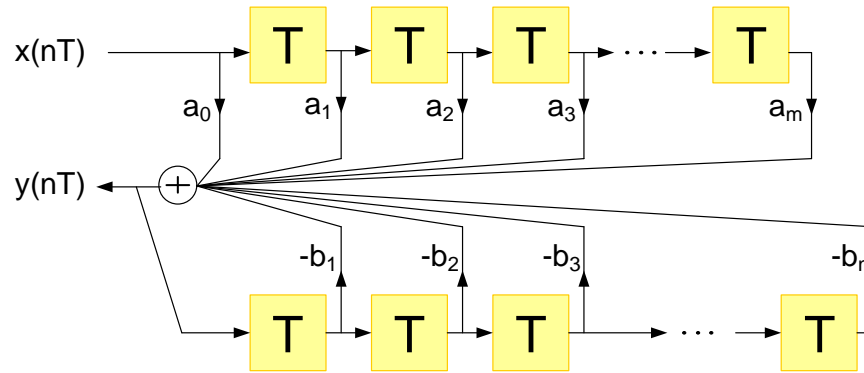
Review from last lecture

Alternate Implementations of an FIR Digital Filter



Review from last lecture

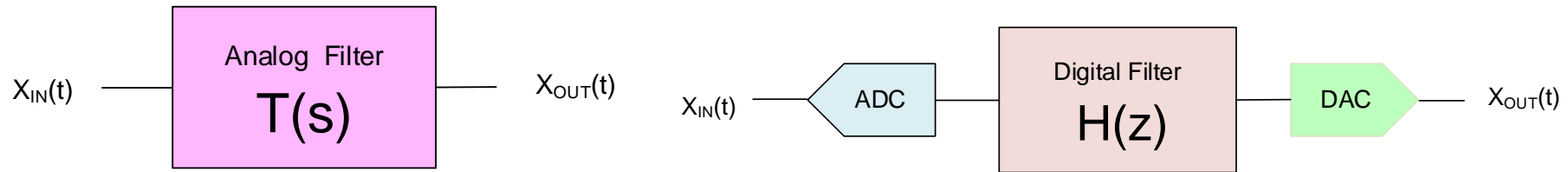
Alternate Implementations of IIR Digital Filter



Excessive delay elements but not of as much concern as excessive Integrators

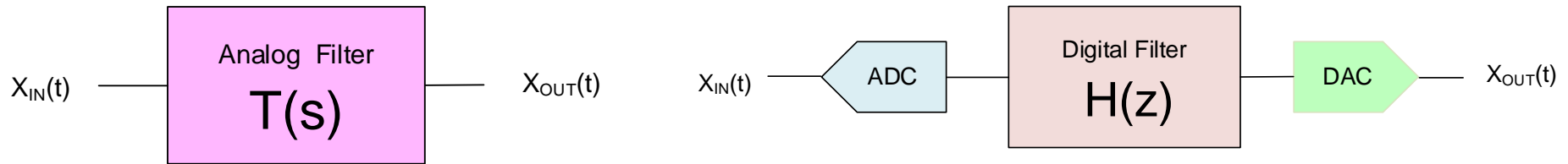
Review from last lecture

Does Digital Filter Overcome Limitations



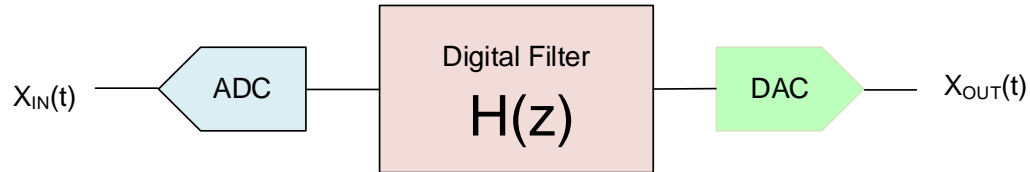
- A - Transfer functions sensitive to component and process variations
- D - Transfer function part of $H(z)$ not sensitive to process variations
 - Transfer function sensitive to coefficient quantization
 - ADC and DAC minimally sensitive to process variations but highly sensitive to mismatch
- A - Distortion inherent due to nonlinearities in components (particularly amplifiers)
- D - Transfer function part of $H(z)$ not sensitive nonlinearity of components
 - ADC and DAC sensitive to nonlinearity of components
- A - Power dissipation can be large
- D - Power dissipation can be large due to a large number of arithmetic operations during each clock cycle
 - ADC and DAC dissipate considerable energy for high resolution or high speed

Does Digital Filter Overcome Limitations



- A - Area gets large, often unacceptably so for very low frequency poles and even of concern for audio-frequency poles
- D - Area for DSP in Digital Filter can be large
 - ADC and DAC can become large if high resolution is required
 - No area penalty for low frequency operation of digital system
- A - Programmability introduces considerable complexity (with existing approaches)
- D - Programmability of filter characteristics is very efficient with digital filter approach
- A - Making minor changes in filter requirements often necessitates a major redesign effort
- D - Making minor or even major changes in filter requirements requires minimal effort with digital filter approach

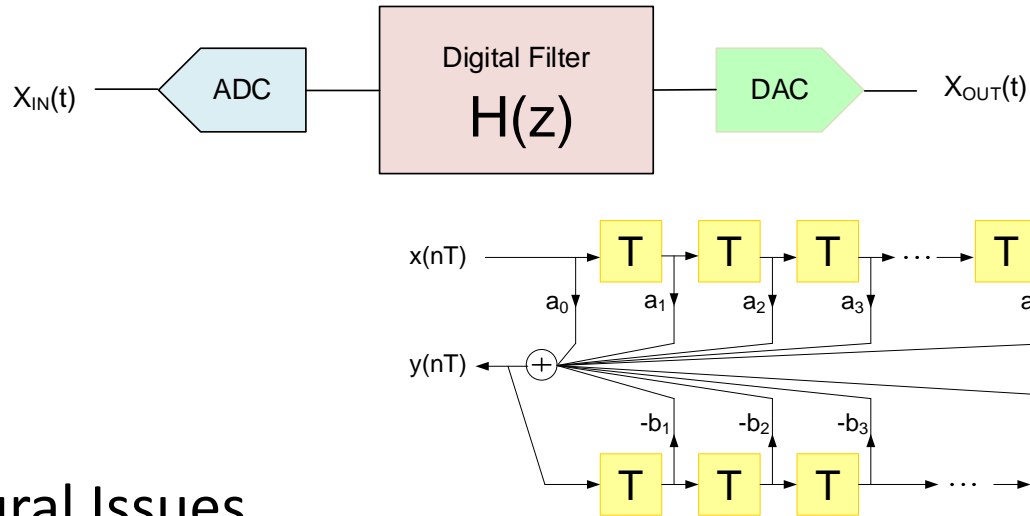
Digital Filter Design Issues



Order of Digital Filters Can be Large

- 128 or more delay elements are not uncommon
- Can achieve very steep transitions from passband to stop band
- High Q poles can be practically realized
- Particularly attractive for filtering low-frequency signals
- Large number of adds and multiplies slows response of the filter
- ARMA filters invariably are of lower order than FIR filters for given transition requirements
- FIR filters inherently stable

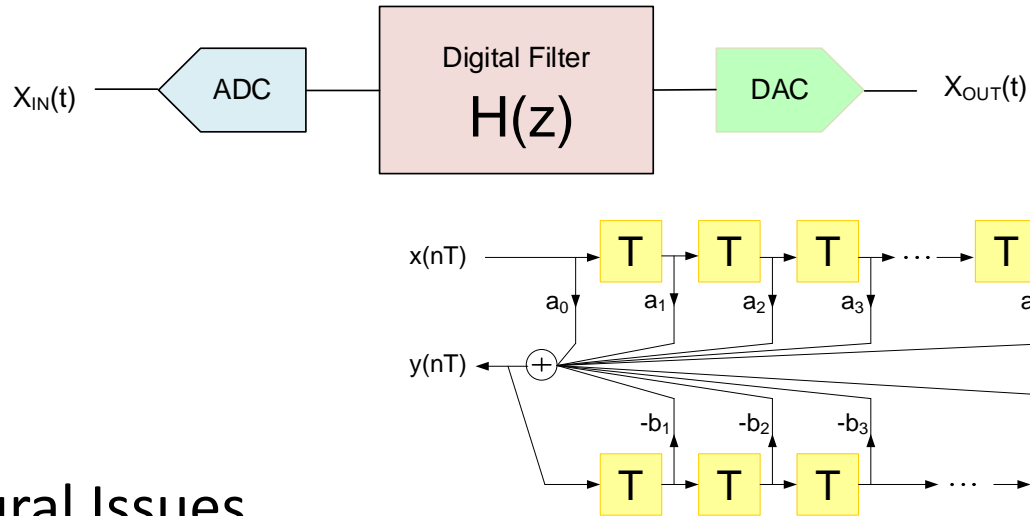
Digital Filter Design Issues



Architectural Issues

- Many different filter architectures
- Must be sure to not overflow registers during intermediate calculations
- Order of operations for given architecture can affect performance
- Coefficient sensitivity can be high
- Number of bits of resolution on coefficients affects multiply and add times
- Some work on filters where all coefficients are power of 2 (multiplies become simply shifts)
- Concerns about how many intermediate memory locations are required

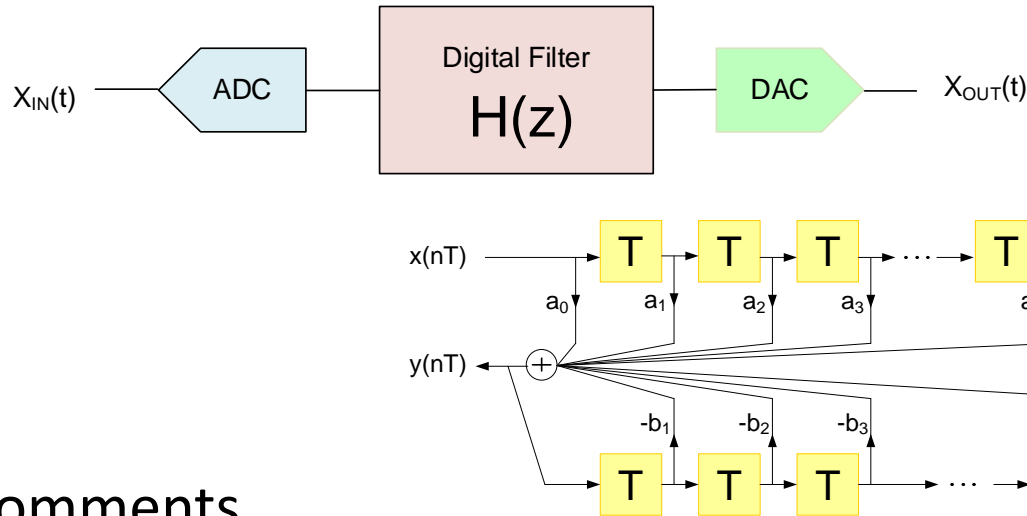
Digital Filter Design Issues



Architectural Issues

- May not be easy to assess overflow concerns without overdesign since intermediate totals dependent upon input
- Architecture affects number of arithmetic operations
- Large number of operations can introduce noise into substrate which of concern with systems with extreme SNR where ADC and DAC are on-chip
- Some architectures and some approximations naturally support parallel operations

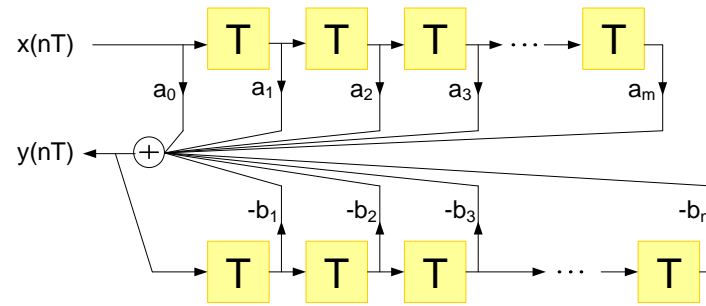
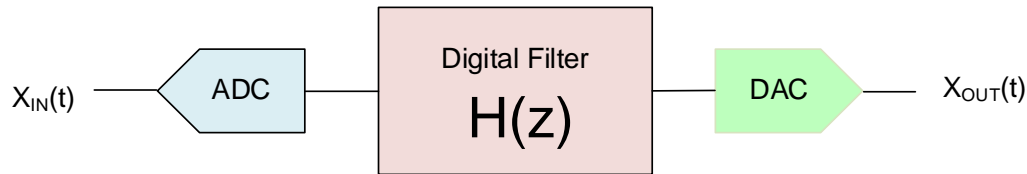
Digital Filter Design Issues



General Comments

- Extreme precision possible with right order and good implementation
- Time and amplitude quantization both affect performance
- Not practical for applications that have very high frequency poles (due to both data converter and filter limitations)
- Power dissipation can be large if many arithmetic operations are required
- May not be easy to assess overflow concerns without overdesign since intermediate totals dependent upon input
- ADC and DAC design efforts can be substantial
- ADC and DAC may require considerable area and power
- Significant effort in design of computer or DSP to drive the digital filter

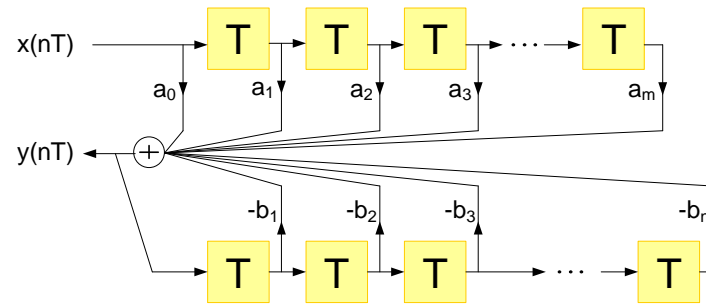
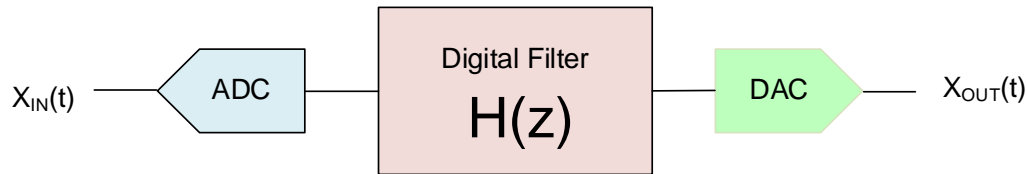
Digital Filter Design Issues



General Comments

- Though process variations in digital filter not of concern, they do affect the ADC and DAC designs beyond matching (e.g. clock skew)
- Big step in area and power to implement the DSP and filter
- Switched Capacitor filters have some properties of a digital filter (time-quantization and thus $H(z)$ instead of $T(s)$) and some of analog filters but overhead for implementing a lower-order filter with SC techniques is relatively small
- DAC often not required since decisions are often made in digital logic and no subsequent analog output is required
- One (of many) applications that favor use of digital filters is in output filtering and decimation in delta-sigma ADCs

Digital Filter Design Issues




General Comments

- Digital filters are vulnerable to aliasing
- Digital filters are expensive
- Digital filters limited to relatively low frequency operation (due to both the data converters and the adds/multiplies)
- Digital filter intermediate results can be stored for later analysis
- The $H(z)$ portion of the digital filter benefits from technology scaling
- The $H(z)$ portion does not drift with time or temperature
- $H(z)$ can be easily tweaked or even modified with software

SECTION 6
DIGITAL FILTERS
Walt Kester

COMPARISON BETWEEN FIR AND IIR FILTERS



IIR FILTERS	FIR FILTERS
More Efficient	Less Efficient
Analog Equivalent	No Analog Equivalent
May Be Unstable	Always Stable
Non-Linear Phase Response	Linear Phase Response
More Ringing on Glitches	Less Ringing on Glitches
CAD Design Packages Available	CAD Design Packages Available
No Efficiency Gained by Decimation	Decimation Increases Efficiency

SECTION 6

DIGITAL FILTERS

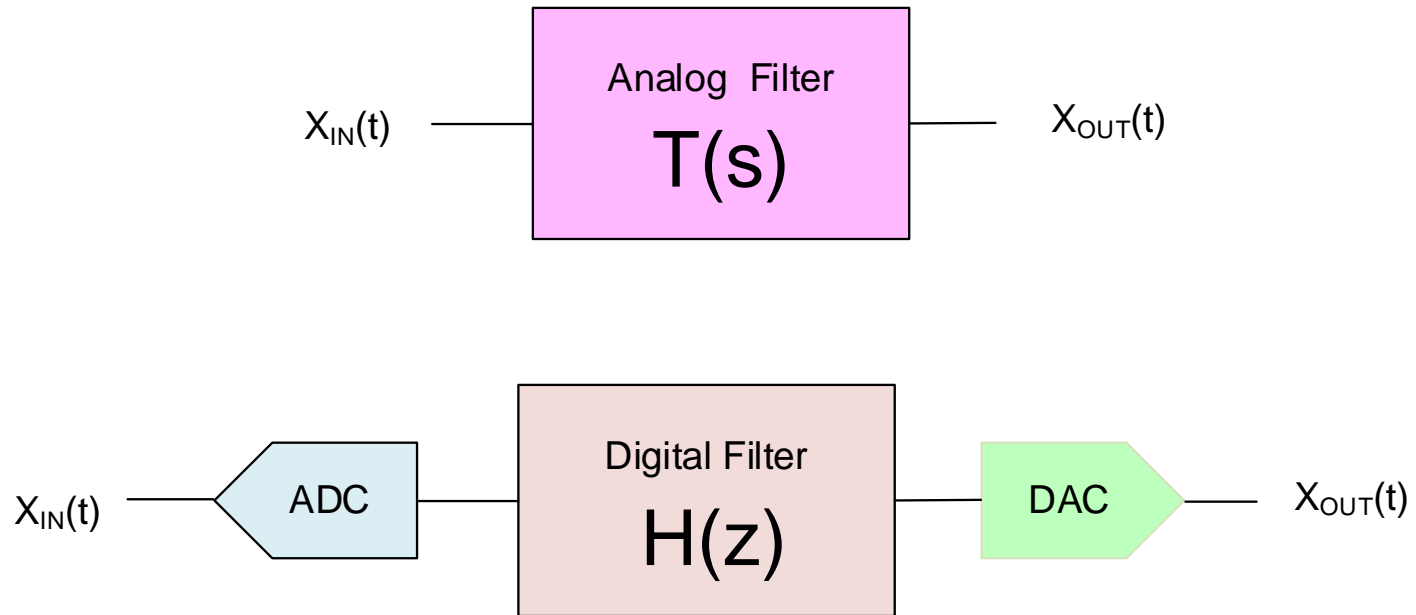
Walt Kester

DIGITAL VERSUS ANALOG FILTERING

DIGITAL FILTERS	ANALOG FILTERS
High Accuracy	Less Accuracy - Component Tolerances
Linear Phase (FIR Filters)	Non-Linear Phase
No Drift Due to Component Variations	Drift Due to Component Variations
Flexible, Adaptive Filtering Possible	Adaptive Filters Difficult
Easy to Simulate and Design	Difficult to Simulate and Design
Computation Must be Completed in Sampling Period - Limits Real Time Operation	Analog Filters Required at High Frequencies and for Anti-Aliasing Filters
Requires High Performance ADC, DAC & DSP	No ADC, DAC, or DSP Required

Figure 6.2

Analog vs Digital Filter



- Both approaches have advantages and limitations
- Digital filters particularly attractive if DSP already available and if ADC and DAC are necessary for other purposes or if decisions in system must be made in the digital domain
- Digital filters also attractive if much of the signal processing will occur in the digital domain of a system
- Digital filters have replaced analog filters in many applications



Stay Safe and Stay Healthy !

End of Lecture 38